

cont.  
B1  
18. (Amended) A semiconductor device according to claim 16 wherein a width of the pair of second regions between the channel forming region and the pair of first regions in said first thin film transistor is different from that of said second and third thin film transistors.

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B2  
20. (Amended) A semiconductor device according to claim 19 wherein said semiconductor film comprises crystalline silicon.

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**REMARKS**

At the outset, the Examiner is thanked for the review and consideration of the present application.

The Examiner's Office Action dated May 23, 2001 has been received and its contents reviewed. Claims 1-25, and 34-41 are pending in the present application, of which claims 1, 6, 11, 16, 19, and 37 are independent.

Referring now to the Office Action, the drawings are objected to for not showing the pairs of second regions being overlapped with the gate electrode, and the multi-layered structure of the gate electrode with the listed metals, which are recited in claims 5, 10, 15, 23, and 30.

With respect to the pairs of second regions being overlapped with the gate electrode, Applicants are submitting herewith corrected Fig. 8A which illustrates overlapping region under gate electrodes of TFT1 and TFT2 highlighted in yellow marker.

With respect to showing the listed metals in the multi-layered structure of the gate electrode, Applicants respectfully submit that the present drawings, such as shown in Fig. 1E, for example, and as recited in claims 5, 10, 15, 23, and 30 are adequate and conventional. Should the Examiner still requires that Fig. 1E be shown with a label for each of the metal, Applicants would do so in a future response.

The specification is objected to as allegedly containing illegible portions on page 12, line 17. In response, Applicants are submitting herewith a copy of the specification including page 12 to permit further review by the Patent Office. No new matter has been added to the copy of the specification.

Claims 17, 18, and 20 are objected to as containing misspellings. Applicants have amended the claims as shown above per the Examiner's suggestion to correct the informalities.

Claims 1-25, and 34-41 are rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Matsumoto (U.S. Patent No. 5,323,042).

Applicants respectfully submit that the pending claims relate to a thin film transistor of a driving circuit that includes a pair of lightly doped regions (i.e. second regions) which are overlapped with a gate electrode. Matsumoto, on the other hand, teaches forming gate electrodes corresponding to the channel regions, as disclosed in col. 3, lines 23-26, and col. 4, lines 60 to line 66.

Applicants respectfully submit that the statement "Gate electrodes 25 to 27 are formed on the respective portions of the upper surface of the gate insulating film 24 each corresponding to the channel regions 21a, 22a, 23a" made by Matsumoto in col. 3, lines 23-26 indicates that there is no overlapping of lightly doped regions with the gate electrodes. As such, Matsumoto is deficient without a cure. Accordingly, the application of Matsumoto in the § 103 rejection is insupportable.

In view of the amendments and arguments set forth above, the objections to the drawings, specification and claims, and the § 103 rejection are respectfully requested to be reconsidered and withdrawn.

### **CONCLUSION**

Having responded to all rejections set forth in the outstanding non-Final Office Action, it is submitted that claims 1-25, and 34-41 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of

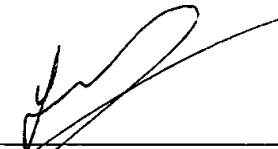
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the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

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VERSION OF AMENDED CLAIMS WITH  
MARKINGS TO SHOW CHANGES MADE

17. (Amended) A semiconductor device according to claim 16 wherein a width of the [par] pair of second regions between the channel forming region and the pair of first regions in said first thin film transistor is within a range from 0.4 to 2  $\mu\text{m}$ .

18. (Amended) A semiconductor device according to claim 16 wherein a width of the [par] pair of second regions between the channel forming region and the pair of first regions in said first thin film transistor is different from that of said second and third thin film transistors.

20. (Amended) A semiconductor device according to claim 19 wherein said semiconductor film comprises [crystal] crystalline silicon.